CLAIMS

1. A metal oxide semiconductor (MOS) integrated device comprising:

a substrate of a first conductivity type, said substrate including a plurality of active zones and inactive zones, said active zones including elementary MOS cells alternating with a plurality of separation zones, each one of said elementary MOS cells including at least one source region, at least one drain region and at least one gate structure, said at least one gate structure including at least one first conductor material finger;

first metal stripes for contacting said source regions of the active zones;

second metal stripes for contacting the drain regions; and

third metal stripes placed on the inactive zones and for contacting said at least one conductor material finger of each elementary cell by forming a contact point formed by a first prolongation of said at least one finger for connecting with one of said third stripes, said first metal stripes, said second metal stripes and said third metal stripes being placed on the substrate substantially at the same level,

wherein at least one of said third metal stripes includes at least one fourth metal stripe placed on one of said separation zones, at least one conductor material finger of each elementary cell having at least one second prolongation and said at least one fourth metal stripe having at least one first prolongation for being placed on said at least one second prolongation of said at least one material conductor finger to form at least another contact point.

2. The device according to claim 1, wherein each separation zone of said plurality of separation zones is alternated to a couple of elementary MOS cells in each active zone.

3. The device according to claim 2, wherein said second metal stripes comprise at least one further metal stripe, said at least one fourth metal stripe being parallel to said at least one further metal stripe and being placed between two of said first stripes.

4. The device according to claim 3, wherein said semiconductor device comprises a lateral diffusion MOS (LDMOS) device and said elementary MOS cells

comprises LDMOS cells, and said substrate comprises an epitaxial layer of the first conductivity type that comprises a plurality of sinker regions of the first type of conductivity and a body region of the first type of conductivity, each body region being placed on each sinker region and includes two of said source regions of said elementary LDMOS cells, each one of said plurality of separation zones being constituted by the portion of the body region between the source regions.

5. The device according to claim 4, wherein said at least one fourth metal stripe extends in a transversally with respect to the formation of the channel of each elementary LDMOS cell.

6. The device according to claim 5, wherein said at least a first prolongation of said at least a fourth stripe and said at least a second prolongation of the conductor material finger extend in a direction parallel to the direction of the channel in each elementary LDMOS cell.

7. The device according to claim 4, further comprising a field oxide layer placed in said one separation zone, said at least a fourth metal stripes being superimposed on said field oxide layer.

8. The device according to claim 7, further comprising a passivant layer placed between said field oxide layer and said at least a fourth metal stripe.

9. The device according to claim 8, wherein said at least one first prolongation of said at least a fourth stripe and said at least a second prolongation of the conductor material finger are placed on body regions of said semiconductor device.

10. The device according to claim 9, further comprising a second prolongation of said at least a fourth stripe and a further prolongation of the conductor material finger which are placed together in said active zones of the device.

11. The device according to claim 1, wherein said conductor material finger comprises a polysilicon finger.

12. The device according to claim 1, wherein said at least a fourth metal stripe

comprises a plurality of fourth metal stripes placed respectively on each one of said separation zone plurality.

13. The device according to claim 12, wherein each one of said third metal stripes comprises said plurality of fourth metal stripes.

14. The device according to claim 1, wherein the active zones of said plurality of active zones of the device are placed adjacent to each other.

15. The device according to claim 14, wherein said second metal stripes further comprise main metal stripes parallel to each other and placed parallel to the formation of the channel of the elementary MOS cells, said main stripes being placed in inactive zones of the device and each couple of adjacent active zones being placed between two of said further main metal stripes.

16. The device according to claim 15, wherein at least one of the further main metal stripes of a couple of active zones is integral with the further metal stripes of the adjacent couple of active zones.

17. The device according to claim 16, further comprising first elements for connecting two further main stripes of each couple of active zones, said first elements being placed on peripheral parts of the chip wherein the device is formed and being associated with first pads for introducing or outputting electric signals.

18. The device according to claim 17, wherein said third metal stripes are parallel to each other and to said further metal stripes and wherein each couple of adjacent active zones comprises one of said second metal stripes that is placed between said two active zones of the couple.

19. The device according to claim 18, further comprising second elements for connecting two third stripes of adjacent couples of active zones, said second elements being placed on peripheral parts of the chip wherein the device is formed and being associated with second pads for introducing or outputting electric signals.

20. The device according to claim 19, wherein said first elements and said first pads are placed in the peripheral part of the chip which opposite to the peripheral

part of the chip wherein said second elements and said second pads are placed.

21. A process for manufacturing a metal oxide semiconductor (MOS) integrated device on a substrate of semiconductor material of a first conductivity type, said process comprising:

forming active zones in said substrate;

forming source regions of a second conductivity type inside said substrate, drain regions of the second conductivity type and gate structures including at least one layer of conductor material, said gate structures forming with the source regions and the drain regions a plurality of elementary MOS cells of said device;

forming a plurality of separation zones alternating with said elementary MOS cells;

masking and depositing a metal layer on said semiconductor substrate in order to form first metal stripes for contacting the source regions, second metal stripes for contacting the drain regions and third metal stripes for contacting each conductor material layer of said gate structures at a point,

wherein the formation of a mask and the deposition of said conductor material of the gate structures allows the formation of first prolongations of said conductor material and wherein the formation of a mask provided with windows on said separation zones for depositing metal in order to form fourth metal stripes connected with said third metal stripes and first prolongations of said fourth metal stripes being placed on said first prolongation of said conductor material in order to form another contact point.

22. The process according to claim 21, further comprising the formation of body regions of the first conductivity type, wherein in each one two source regions of the second conductivity type are formed, each one of said separation zones being constituted by the portion of body region between said two source regions.

23. The process according to claim 22, further comprising the formation of a field oxide layer on each one of said separation zones, each one of said fourth metal stripes being placed on said field oxide layer.

24. The process according to claim 23, further comprising the formation of a passivant layer on each field oxide layer, each one of said fourth metal stripes being placed on said passivant layer.

25. The process according to claim 21, wherein said conductor material layers comprise polysilicon layers.